A DIGITAL ASYNCHRONOUS SAMPLE-RATE CONVERTER FOR DIGITAL VIDEO SIGNALS

Dietmar Wenzel and Joachim Speidel
Institute of Telecommunications
University of Stuttgart
Pfaffenwaldring 47, D-70569 Stuttgart, Germany

ABSTRACT

In this paper, a new all-digital asynchronous sample-rate converter (SRC) for video signals with an effective resolution of 12 bits using digital signal processing is presented. It is designed for the high quality requirements that exist in professional equipment for CATV head ends. The architecture of the digital SRC which is optimized for an implementation with small memory and low processing power is shown in detail. Furthermore, the design of the building blocks is illustrated and the results of a simulation on bit level are presented.

1. INTRODUCTION

Up to now most TV networks have been using analog techniques for transmitting, distributing and storing video signals. More and more, particularly in TV studios, digital techniques are preferred [1, 2, 3, 4]. The most important parameter of a digital signal is its sampling frequency which mostly depends on the digital system processing the signal. Often, the standardized sampling frequency $f_{S,1} = 13.5$ MHz is used for color video blanking and synchronizing signals (CVBS signals) according to the ITU color television standard [2, 5]. Therefore, problems will arise if such signals are fed directly into digital transmission or storing systems working with a different and asynchronous sampling frequency $f_{S,2}$ in comparison to the signal source. Consequently, an asynchronous sample-rate converter is needed for the interface [6]. A straight forward solution would be the use of a D/A converter operating with $f_{S,1}$ which is connected to an A/D converter operating with the new sampling frequency $f_{S,2}$ (Fig. 1). To attenuate the unwanted spectral parts at $n \cdot f_{S,1}$, $n = \pm 1, \pm 2, \ldots$ and to satisfy the sampling theorem for the sampling frequency $f_{S,2}$ a lowpass filter with a cut-off frequency

$$f_{LP} = \tfrac{1}{2}\min\left\{f_{S,1}, f_{S,2}\right\} \tag{1}$$

is required. It operates as reconstructing and anti-aliasing filter, simultaneously. However, this method suffers from all known disadvantages of analog signal processing. Therefore, an all-digital solution is preferred [7, 8].

In recent years, asynchronous SRCs have been designed for audio signals [9, 10, 11]. In contrast, video signals have a higher bandwidth but require a smaller word length. With todays digital technology an implementation is possible.

Fig. 2 (top) shows the functional block diagram of the digital asynchronous sample-rate conversion. First, the input signal $x(m)$ with sampling frequency $f_{S,1}$ is interpolated by a factor L using the upsampler and the anti-image filter H_{SRC} with cut-off frequency $\Omega_{LP} = 2\pi f_{LP}$ and stopband attenuation $1/\delta_S$. The output are samples on a time base which is L times faster in comparison to the input signal. Each sample is latched in a hold circuit until it is substituted by its successor. As shown in Fig. 2 (bottom), the hold circuit implements the transition from the discrete-time signal into a step shaped continuous-time signal $\ddot{y}(t)$. Finally, this signal is sampled with the output sampling frequency $f_{S,2}$. However, for large values of L it is almost not possible to calculate every output sample of the interpolation filter H_{SRC} due to the increased speed requirements of the technology. Therefore, an efficient solution calculating only those samples needed for the output signal $y(n)$ is presented in this paper.

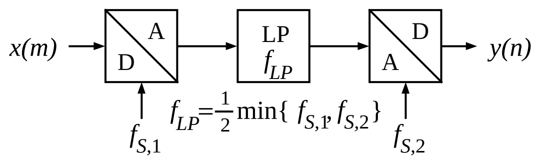

Fig. 1. Analog asynchronous sample-rate converter

2. PRECONDITIONS

For the design of the SRC it is necessary to define some preconditions:

- Both sampling frequencies $f_{S,1}$ and $f_{S,2}$ shall satisfy the sampling theorem

$$f_{S,1} > 2 f_C \text{ and } f_{S,2} > 2 f_C \tag{2}$$

where f_C is the cut-off frequency of the original analog signal $x(t)$.

- Especially, for the input sampling frequency $f_{S,1}$
$$f_{S,1} = 2\,b\,f_C\,, \quad b > 1 \tag{3}$$
holds. b is the oversampling factor. For the standardized sampling frequency $f_{S,1} = 13.5\,\text{MHz}$ and a video signal with $f_C = 5\,\text{MHz}$ $b = 1.35$ results. The higher b the less complex the filter H_{SRC} has to be.

- In this paper, for the design of the SRC we assume
$$f_{S,2} = \tfrac{2}{11}\cdot 155.52\ \text{MHz} \approx 14.14\ \text{MHz}\,. \tag{4}$$
Obviously, $f_{S,2}$ is derived from the synchronous digital hierarchy (SDH) which is used for the transmission of the video signal in the TV network mentioned in section 1. This clock signal is asynchronous to the sampling clock with frequency $f_{S,1}$. Thus, for the frequency ratio k we obtain
$$k = f_{S,2}/f_{S,1} \approx 1.0473\,. \tag{5}$$

- The SRC should have an effective resolution for the output signal of
$$w \approx 12\ \text{bits} \tag{6}$$
which corresponds to an SNR of about 73 dB, respectively. Thus, the mean power N_{SRC} of the error caused by the SRC should not be higher than the power N_Q of the quantization error for the signal $x(m)$ quantized with w bits.

3. Interpolation filter for the SRC

3.1. Requirements

For the input signal $x(m)$ of the SRC in frequency domain
$$X\left(e^{j\Omega'}\right) = \sum_{m=-\infty}^{\infty} x(m)\cdot e^{-jm\Omega'} \ \text{ with } \ \Omega' = 2\pi\frac{f}{f_{S,1}} \tag{7}$$
holds. For the output signal of the interpolation filter H_{SRC}, we obtain
$$X_{SRC}\left(e^{j\Omega''}\right) = X\left(e^{jL\Omega''}\right)\cdot H_{SRC}\left(e^{j\Omega''}\right),\ \Omega'' = \Omega'/L\,. \tag{8}$$
The output of the hold circuit is $\tilde{y}(t)$ and is given in frequency domain by
$$\tilde{Y}(\Omega'') = X\left(e^{jL\Omega''}\right)\cdot H_{SRC}\left(e^{j\Omega''}\right)\cdot \mathrm{si}(\Omega''/2) \tag{9}$$
where $\mathrm{si}(x) = \sin(x)/x$. If we scale with response to the output sampling frequency $f_{S,2}$ it is

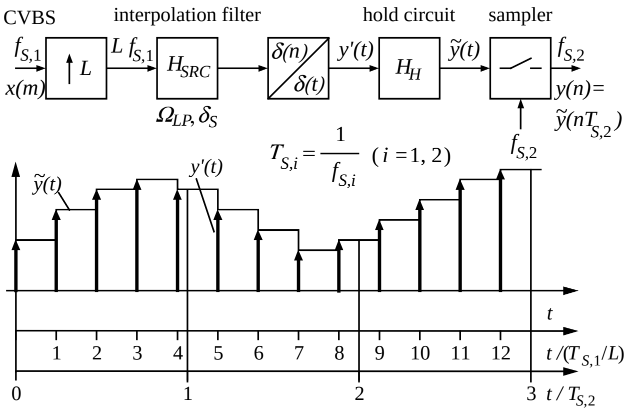

Fig. 2. Principle of digital asynchronous sample-rate conversion

$$\tilde{Y}(\Omega k/L) = X\left(e^{j\Omega k}\right)\cdot H_{SRC}\left(e^{j\Omega k/L}\right)\cdot \mathrm{si}\left(\tfrac{\Omega k}{2L}\right) \tag{10}$$
with $\quad \Omega = 2\pi\dfrac{f}{f_{S,2}}$, $\Omega = \Omega''\dfrac{L}{k}$ and $k = \dfrac{f_{S,2}}{f_{S,1}}$.

If we use the normalized sampling function in the frequency domain
$$D_{f_{S,2}}(\Omega) = 2\pi\sum_{\mu=-\infty}^{\infty}\delta(\Omega - 2\pi\mu)\,, \tag{11}$$
we obtain the spectrum of the output signal $y(n)$
$$\begin{aligned} Y\left(e^{j\Omega}\right) &= \frac{1}{2\pi}\int_{-\infty}^{\infty}\tilde{Y}(\nu\,k/L)\cdot 2\pi\sum_{\mu=-\infty}^{\infty}\delta(\Omega - 2\pi\mu - \nu)\,d\nu \\ &= \sum_{\mu=-\infty}^{\infty} X\left(e^{j(\Omega-2\pi\mu)k}\right)\cdot H_{SRC}\left(e^{j(\Omega-2\pi\mu)k/L}\right) \\ &\qquad \cdot \mathrm{si}\left(\tfrac{1}{2}(\Omega - 2\pi\mu)k/L\right) \\ &= \sum_{\mu=-\infty}^{\infty} X\left(e^{j\Omega k}\ e^{-j2\pi\mu k}\right)\cdot H_{SRC}\left(e^{j\Omega k/L}\ e^{-j2\pi\mu k/L}\right) \\ &\qquad \cdot \mathrm{si}\left(\tfrac{1}{2}(\Omega - 2\pi\mu)k/L\right). \end{aligned} \tag{12}$$
It is obvious from equation (12) that the spectrum of the output signal $y(n)$ is periodic and that the sample-rate conversion by factor k is achieved due to the factor k in the exponent of the argument on the right side. For the synchronous case $k = L$ holds and equation (12) becomes
$$Y\left(e^{j\Omega}\right) = X\left(e^{jL\Omega}\right)\cdot H_{SRC}\left(e^{j\Omega}\right)\cdot \underbrace{\sum_{\mu=-\infty}^{\infty}\mathrm{si}\left(\tfrac{1}{2}(\Omega - 2\pi\mu)\right)}_{=1}. \tag{13}$$

The reasons for the error caused by the SRC are: The filter H_{SRC} has a finite attenuation and due to the discrete-time processing a periodic magnitude response with period $Lf_{S,1}$. Fig. 3 clarifies these facts. The spectral components around $i\cdot Lf_{S,1}$, $i = \pm1, \pm2, \ldots$ are not attenuated by the filter H_{SRC}. Only the magnitude response of the hold circuit

$$H_H(f) = \mathrm{si}\left(\pi f / \left(L f_{S,1}\right)\right) \tag{14}$$

attenuates those spectral parts. Due to the sampling with $f_{S,2}$, these residual spectral components interfere with the wanted part of the spectrum in the frequency range $|f| \le f_C$ according to (12).

For a sinusoidal input with frequency f_C and amplitude A

$$x(m) = A \cdot \sin\left(2\pi m\, f_C / f_{S,1}\right) \tag{15}$$

we obtain the maximum average distortion power according to Fig. 3a

$$\begin{aligned} N_H &= \left(\frac{A f_{S,1}}{2}\right)^2 \sum_{\substack{i=-\infty \\ i\neq 0}}^{+\infty} \left[H_H^2\left(iLf_{S,1} - f_C\right) + H_H^2\left(iLf_{S,1} + f_C\right)\right] \\ &= \frac{1}{2}\left(A f_{S,1}\right)^2 \cdot \\ &\quad \sum_{i=1}^{\infty}\left[\frac{\sin^2\left(\pi\left(i - \frac{f_C}{Lf_{S,1}}\right)\right)}{\pi^2\left(i - \frac{f_C}{Lf_{S,1}}\right)^2} + \frac{\sin^2\left(\pi\left(i + \frac{f_C}{Lf_{S,1}}\right)\right)}{\pi^2\left(i + \frac{f_C}{Lf_{S,1}}\right)^2}\right] \\ &\approx \left(\frac{A f_C}{L}\right)^2 \cdot \sum_{i=1}^{\infty}\frac{1}{i^2} = \frac{\pi^2}{6}\left(\frac{A f_C}{L}\right)^2 . \end{aligned} \tag{16}$$

Since the simplifications $|\sin(i\pi \pm x)| \approx |x|$ and $i \pm x \approx i$ can be used for $|x| << 1$, the approximation holds for $f_C << L f_{S,1}$. Considering the average signal power $S = A^2 f_{S,1}^2 / 2$ we obtain the signal-to-noise ratio (SNR)

$$\frac{S}{N_H} = \frac{3}{\pi^2}\left(\frac{L f_{S,1}}{f_C}\right)^2 \tag{17}$$

As it can be shown in a similar way which is not done herein, the SNR for a discrete-time signal with constant amplitude density spectrum $A f_{S,1}$ in the frequency range $|f| < f_C$ and null in the frequency range $f_C \le |f| \le f_{S,1}$ is 3 times higher than in (17) (Fig. 3b).

If we consider the equivalent noise bandwidth of the hold circuit in the case of white noise

$$f_{eq} \approx \int_0^{\infty}\left|H_H^2(f)\right| df = \int_0^{\infty} \mathrm{si}^2\left(\pi \frac{f}{L f_{S,1}}\right) df = L\frac{f_{S,1}}{2}, \tag{18}$$

we find that f_{eq} is L times higher than the maximum cut-off frequency $f_{C,\max} = f_{S,1}/2$ of the signal. Further, if we assume that the magnitude response in the stop band of the interpolation filter H_{SRC} is a constant δ_S which

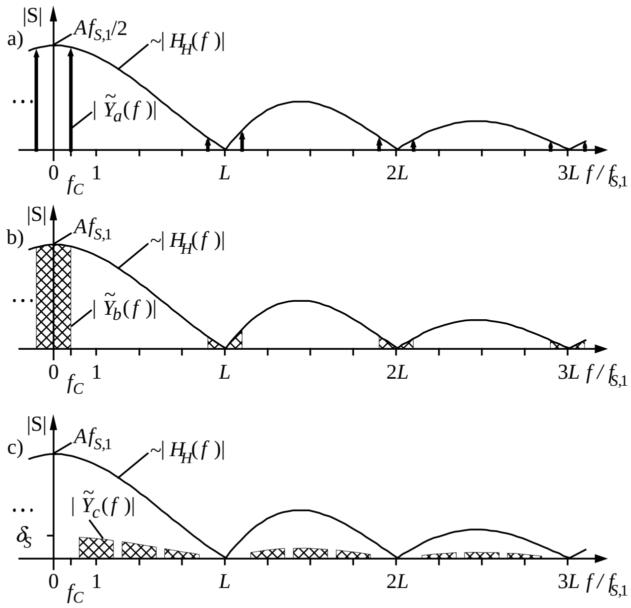

Fig. 3. Influence of the hold circuit on periodic spectral components of a sinusoidal signal (a), of a signal with constant spectral density which are not attenuated by the interpolation filter (b) and which are attenuated (c)

is weighted by $|H_H(f)|$ (Fig. 3c), the ratio between the wanted part S and the unwanted part N_S is

$$S/N_S = 1/\left(L\delta_S^2\right). \tag{19}$$

Then, the total error power is $N_H + N_S$ which should not be higher than the power N_Q of the quantization error for the signal $x(m)$ quantized with w bits (section 2). The SNR for a sinusoidal signal quantized with w bits is

$$S/N_Q\big|_{dB} = 10\,\lg\left(3\cdot 2^{2w-1}\right) \approx w \cdot 6.02\text{ dB} + 1.76\text{ dB}. \tag{20}$$

Since the SNR from (17) should be higher than the SNR from (20) the interpolation factor L is given by

$$L > 2^{w-1/2}\pi\frac{f_C}{f_{S,1}}. \tag{21}$$

For the values used in section 2, $L \ge 3370$ holds. If we take into account the finite attenuation of the filter H_{SRC} in its stop band, we have to postulate using (19):

$$\frac{2^{-2w+1}}{3} > \frac{\pi^2}{3}\left(\frac{f_C}{L f_{S,1}}\right)^2 + L\delta_S^2 . \tag{22}$$

Therefore, we obtain the inequality for δ_S

$$\delta_S < \sqrt{\frac{1}{3L}\left(2^{-2w+1} - \left(\pi\frac{f_C}{L f_{S,1}}\right)^2\right)} . \tag{23}$$

For an efficient design we choose

$$L = 4096 = 2^{12}\,. \tag{24}$$

Again, using the values from section 2, we obtain from (23) a minimum constant stopband attenuation

$$-20\lg\delta_S = 115\,\mathrm{dB}\,. \tag{25}$$

It is advantageous if $N_H \approx N_S$ holds. This is achieved if

$$\delta_S \approx \frac{\pi}{\sqrt{3}}\frac{f_C}{f_{S,1}}L^{-3/2} \tag{26}$$

and is accomplished very well by the values according to (24) and (25).

3.2. DESIGN

In order to reduce the overall number of coefficients and to reduce the processing power it is helpful to split the filter H_{SRC} into a cascade of various filters performing the interpolation of the signal in several stages. Therefore, most filters of the cascade can operate at a lower sampling frequency than $f_{S,2}$ and we can profit from the benefits of half-band filters, M-band filters, multi-rate signal processing and polyphase filter structures. A good approach is to split the interpolation factor into 3 subfactors

$$L = 4096 = L_1 \cdot L_2 \cdot L_3 = 2 \cdot 2 \cdot 1024 \tag{27}$$

so that we can write

$$H_{SRC}\left(e^{j\Omega}\right) = 2^{12} \cdot H_1\left(e^{j2048\Omega}\right) \cdot H_2\left(e^{j1024\Omega}\right) \cdot H_3\left(e^{j\Omega}\right)\,. \tag{28}$$

For the first and second stages we can employ half-band filters whereas for the third stage a M-band filter with 1023 separate uniformly spaced stop bands is required. For the design of the half-band filters the method in [12] is easy to implement and yields good results. With $N_1 = 63$ coefficients for H_1 and $N_2 = 23$ for H_2 a stop band attenuation of approximately 115 dB and passband ripples of less than 0.001 dB are achieved for both filters.

For the design of the M-band filter H_3 the method in [13] is well-suited. This design method uses a LMS approach to minimize the error of the interpolated signal in time domain. The coefficients for the H_3 can be calculated with the following Matlab function [14]:

```
function h = srcf(s, L, R)
% This function designs an FIR filter for
% interpolation of band limited signals by factor L
% considering R samples of the input signal on each
% side of the interpolated value.
% Usage:   h = srcf(s, L, R)
% where s/2L = normalized cut-off frequency, 0<s<1,
%        2RL = length of impulse response,
%          h = resulting impulse response.
% 1. Calculation of matrix for sin(x)/x values:
nm = toeplitz(0:-1:(1-2*R), 0:(2*R-1));
S  = sinc(s*nm);
% 2. Calculation of b for l = 0,..., L-1:
nm = L*[(-R):(R-1)]' * ones(1,L)
     + ones(2*R,1)*[0:(L-1)];
b = sinc((s/L)*nm);
% 3. Calculation of the impulse response:
H = [S\b]';
h = reshape(H, (2*R*L), 1);

function y = sinc(x)
% Calculation of sin(x)/x values for the matrix x:
[m,n] = size(x);
h = zeros(m,n);
for k = 1:m
  for l = 1:n
    if x(k,l) ~= 0
      h(k,l) = sin(x(k,l))/x(k,l);
    else
      h(k,l) = 1;
    end
  end
end
y = h;
```

If we use the parameters s, L and R with

$$s = 0.2\,,\;\; L = L_3 = 1024\,,\;\; R = 3 \tag{29}$$

the finite impulse response $h_3(n)$ with $N_3 = 6144$ coefficients shown in Fig. 4 is obtained.

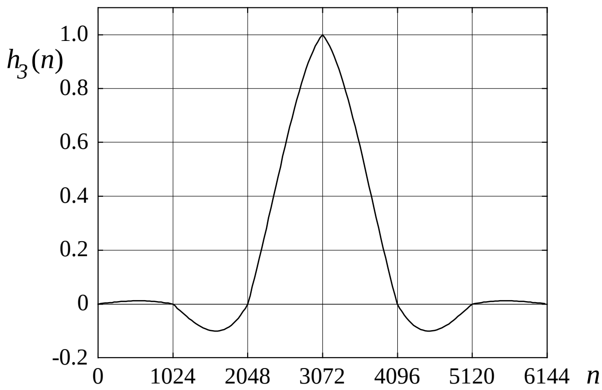

Fig. 4. Impulse response of filter H_3

If we split H_3 into 1024 polyphases only $N_3/1024 = 6$ successive samples of the signal $x'(m')$ in Fig. 5 are needed for the computation of the desired output sample y at time n. Fig. 5 shows the processing architecture if H_3 is split into polyphases

$$h_{3,p(n)}^{(p)}(\mu) = h_3\left(\mu L_3 + p(n)\right), \tag{30}$$

where $0 \le p(n) < 1024$ is the polyphase index of the impulse response $h_3(n)$ that corresponds to the output sample y at time n. The polyphase decomposition of H_1 and H_2 is not shown in Fig. 5. The samples $x'(m')$ are stored in a circular buffer (FIFO). The instant of time when a rising edge of the output clock with frequency $f_{S,2}$ occurs determines which group of 6 samples from $x'(m')$ is required to compute the corresponding output sample. That group is identified by the read index $s(n)$. In addition, the polyphase index $p(n)$ depends on the instant of time of the output sample, too.

Therefore, it is not necessary to compute each sample in the L times faster time base. Fig. 6 visualizes which polyphase of the impulse response has to be chosen to compute the output sample for a specific instant of time

$$y(n) = \sum_{\mu=0}^{5} x'\left(m'[s(n)] - \mu\right) \cdot h_{3,p(n)}^{(p)}(\mu) . \qquad (31)$$

The dependency of $s(n)$ and $p(n)$ on a certain instant of time n is shown in Fig. 7 and will be discussed in section 4.

Fig. 8 shows the magnitude response of H_3 in the frequency range $0 < f < 24 f_{S,1}$. Trace b) is for unquantized coefficients, trace c) for coefficients quantized with 16 bits and trace a) for coefficients quantized with 16 bits and a piecewise linear interpolated impulse response. For the piecewise linear interpolation of the impulse response in case a) only every 32nd sample of the original impulse response $h_3(n)$ is stored in order to save memory. All other coefficients are linearly interpolated in real time. If the symmetry of $h_3(n)$ is exploited, only 96 values, each 16 bits wide, have to be stored instead of 6144 as in case b) or c). For case a) there is only a slight degradation of the stopband attenuation. Nevertheless, the attenuation complies with (25) at any frequency point in all stop bands (shaded).

The overall magnitude response of H_{SRC} according to (28) is shown in Fig. 9 for the frequency range $0 < f < 16 f_{S,1}$. The stop bands induced by H_1, H_2 and H_3 are well defined. The gray areas at the top of Fig. 9 are a schematic representation of the upsampled signal spectrum.

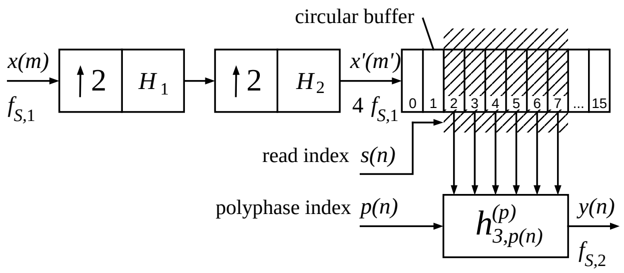

Fig. 5. Structure of the SRC with 3 stages

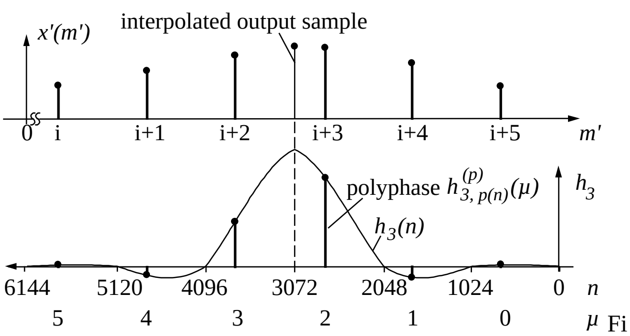

Fig. 6. Computation of an output sample using one polyphase component of H_3

4. SAMPLING FREQUENCY RATIO DETECTION

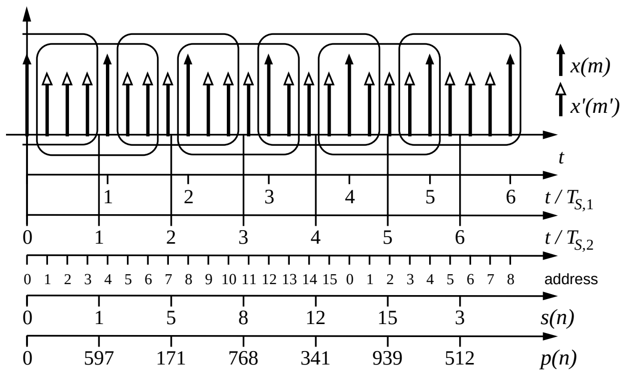

Fig. 7. Relation between address, read index and polyphase index

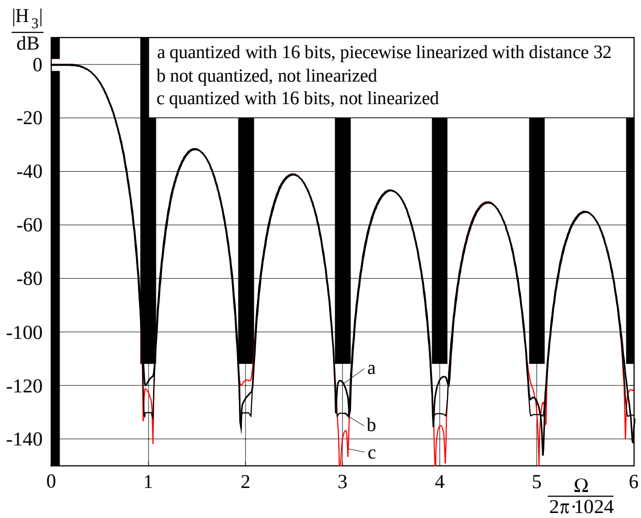

Fig. 8. Magnitude response of H_3 (segment)

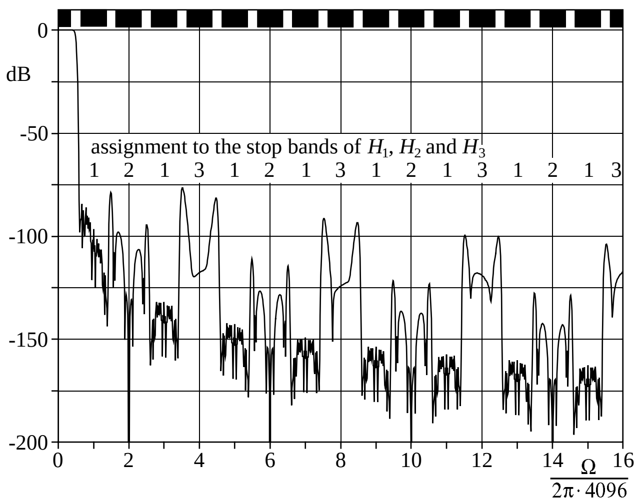

Fig. 9. Magnitude response of H_{SRC} (segment)

In order to determine the correct value of the read index $s(n)$ and the polyphase index $p(n)$ for a certain instant of time n, it is necessary to know the actual ratio k of the sampling frequencies defined in (5). Particularly, we have to know which sample of the L possible samples between $x(m)$ and $x(m+1)$ has to be computed. Fig. 10 shows that this information can be deduced from the input and output clock.

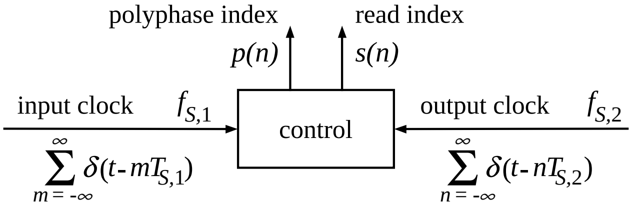

Fig. 10. Controlling of the polyphase index and read index

If we assume that the ratio k only varies very slowly with time, then we can employ an all-digital phase locked loop (PLL) as shown in Fig. 11 in order to determine the ratio k in relative short time and with high precision. The advantage of this method is that no part of the SRC operates with a clock frequency higher than $2 f_{S,1}$.

The PLL tracks the phase $\varphi_1'(m)$ of the input clock and controlls the phase $\varphi_2(n)$ of the oscillator. In case of an all-digital PLL only the phase accumulator of a numerically controlled oscillator (NCO) is necessary to implement this operation. The sine-wave output of the NCO is not needed. If the PLL operates with the output sampling frequency $f_{S,2}$ and is locked and settled, the phase increment κ^{-1} in Fig. 11 equals to the ratio k^{-1}. The read index $s(n)$ and the polyphase index $p(n)$ can easily be deduced from the phase $\varphi_2(n)$.

The phase $\varphi_1'(m)$ of the input clock is represented by the value of a Gray code counter clocked with $f_{S,1}$.

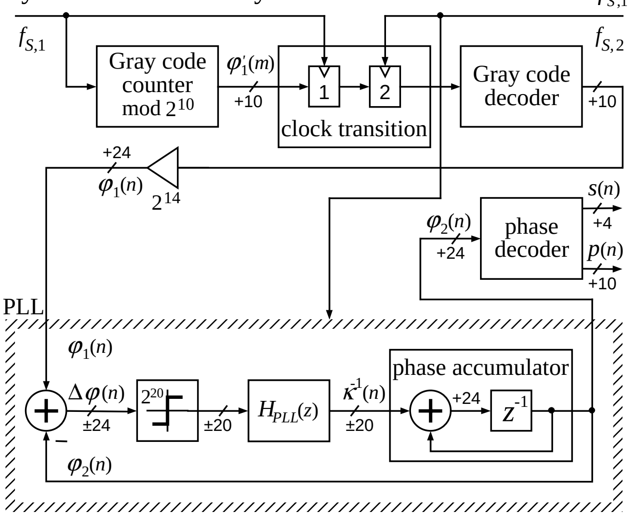

Fig. 11. Block diagram of the all-digital PLL

In order to compare this phase with the phase $\varphi_2(n)$, $\varphi_1'(m)$ has to be converted to the output time base. This transition is carried out by the block "clock transition" in Fig. 11 containing two registers. Usually, if the value from register 1 is taken into register 2 at the same instant of time while the value of register 1 is changing an error might occur. Since a Gray code is used, even in this case the new value in register 2 is valid. After Gray decoding the value is multiplied by the constant 2^{14}. This yields a higher resolution for the phase difference

$$\Delta\varphi(n) = \varphi_1(n) - \varphi_2(n). \tag{32}$$

Anyway, because of the interpolation factor L from (24) a resolution of at least 2^{12} is necessary. Due to the limited word length of the Gray counter and of the phase accumulator overflows occur periodically. Usually, $\Delta\varphi(n)$ is very small, but in these cases $\Delta\varphi(n)$ can become very large. To avoid disturbances of the settled state of the PLL and to avoid overflows in the loop filter H_{PLL}, a limiter keeps $|\Delta\varphi(n)|$ to a maximum of 2^{20} before the signal is fed into the loop filter. But, the threshold of the limiter should be high enough so that it is not limiting during the settling time of the PLL.

The task of the loop filter H_{PLL} is to attenuate high frequency noise in $\Delta\varphi(n)$. The lower the cut-off frequency of H_{PLL} the more precise is the average value of phase increment κ^{-1}. The loop filter consists of a first order IIR filter followed by an integrator [10] (Fig. 12). To achieve a fast settling of $\kappa^{-1}(n)$ and a low noise value after settling the PLL can switch between two filter characteristics. Depending on the magnitude of $\Delta\varphi(n)$ a comparator decides whether the output signal of filter IIR1 or IIR2 is used. Using the coefficients from Tab. 1, we can write in *z* domain

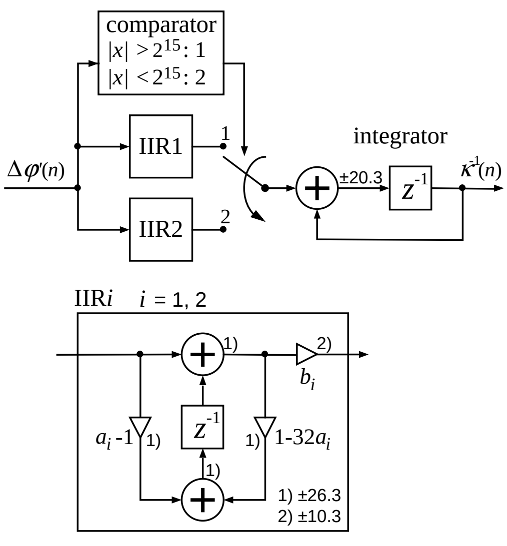

Fig. 12. Block diagram of the loop filter H_{PLL}

$$H_{PLL,i}(z) = b_i \, \frac{1-(1-a_i)\, z^{-1}}{1-(1-32a_i)\, z^{-1}} \cdot \frac{z^{-1}}{1-z^{-1}}\,, \; i = 1, 2\,. \quad (33)$$

Tab. 1 Coefficients of the loop filter H_{PLL}

i	a_i	b_i
1	2^{-8}	2^{-8}
2	2^{-11}	2^{-15}

The phase transfer function of the open loop control is

$$\Phi_{O,i}(z) = \left. \frac{Z\{\varphi_2(n)\}}{Z\{\varphi_1(n)\}} \right|_{open} = H_{PLL,i}(z) \cdot \frac{z^{-1}}{1-z^{-1}}\,. \quad (34)$$

Therefore, we obtain for the phase transfer function of the closed loop control

$$\Phi_{C,i}(z) = \left. \frac{Z\{\varphi_2(n)\}}{Z\{\varphi_1(n)\}} \right|_{closed} = \frac{\Phi_{O,i}(z)}{1+\Phi_{O,i}(z)}\,. \quad (35)$$

The magnitude response of $\Phi_{C,i}$ is shown in Fig. 13. The cut-off frequency Ω_C of the PLL is defined by

$$\left|\Phi_O\left(e^{j\Omega_C}\right)\right| = 1\,. \quad (36)$$

Therewith the PLL is not oscillating, the phase margin

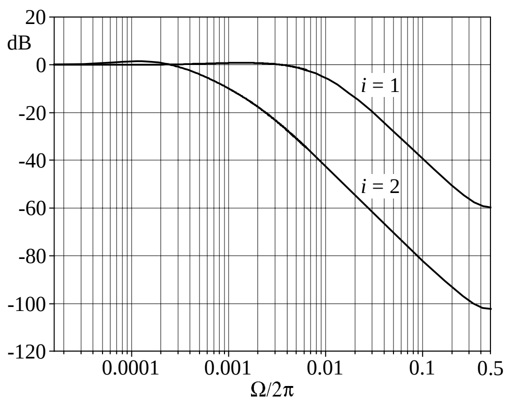

Fig. 13. Magnitude response of the phase transfer function for the closed loop control

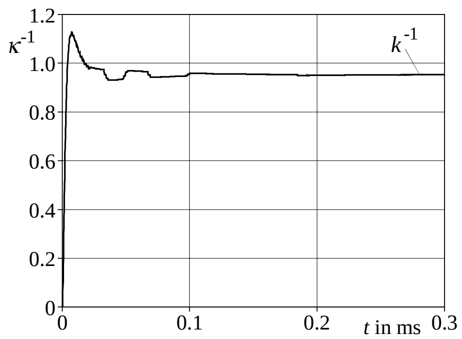

Fig. 14. Transient effect of $\kappa^{-1}(n)$ for the PLL, initial value $\kappa^{-1} = 0$

$$\varphi_R = \mathrm{arc}\left(\Phi_O\left(e^{j\Omega_C}\right)\right) + 180° \quad (37)$$

has to be positive. For the parameters from Tab. 1 φ_R is about 70°. In Fig. 14 the settling of $\kappa^{-1}(n)$ towards k^{-1} is shown. The PLL automatically switches between the two filter characteristics during the transient effect. The settling time is about 0.2 ms.

Due to the fact that the PLL is a discrete system the word lengths of the signal paths have to be adapted to the range of the signals. Detailed investigations have shown that no overflow occurs if the word lengths according to Figs. 11 and 12 are used. The assignment is defined by

$$\begin{aligned} +X &\rightarrow \left[0, 1, \ldots, 2^X - 1\right] \\ \pm X &\rightarrow \left[-2^X, -2^X + 1, \ldots, 2^X - 1\right] \\ \pm X.Y &\rightarrow \left[-2^X, -2^X + 2^{-Y}, \ldots, 2^X - 2^{-Y}\right]. \end{aligned} \quad (38)$$

Finally, the read index $s(n)$ and the polyphase index $p(n)$ can be deduced from the content of the phase accumulator $\varphi_2(n)$ according to the scheme in Fig. 15. The operation of the circular buffer was already shown in Fig. 7. $s(n)$ indicates the address of the first sample of a group used for computation. $p(n)$ corresponds to the instant of time for the output sample.

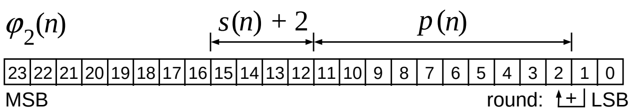

Fig. 15. Decoding the content of the phase accumulator

5. PERFORMANCE

The performance of the SRC is measured in terms of the noise power and distortion which is added to the input signal, e.g., a sine-wave input. The sine-wave is chosen in such a way that its period is an integer multiple K of the output sampling period $1/f_{S,2}$. Using the DFT with length N we obtain for the unweighted THD+N ratio (total harmonic distortion and noise) in the frequency range of interest

$$SNR = 20 \cdot \lg \left| \sum_{n=a}^{a+N-1} y(n) \cdot e^{-j2\pi n \frac{K}{N}} \right| - 10 \cdot \lg \sum_{\substack{\mu=N_L \\ \mu \neq K'}}^{N_U} \left| \sum_{n=a}^{a+N-1} y(n) \cdot e^{-j2\pi \frac{\mu n}{N}} \right|^2 . \quad (39)$$

where $\quad N_L = 0$ and $N_U = N\, f_C / f_{S,2}\,. \quad (40)$

Fig. 16 shows the magnitude response of the sine-wave output with $f \approx 4.13$ MHz for the frequency ratio from (5). The peaks limiting the spurious free dynamic range (SFDR) are caused by the finite attenuation of the interpolation filter, the effect of the hold circuit discussed in subsection 3.1 and the limited accuracy of the PLL. The SFDR is 78.0 dB and the THD+N is 73.1 dB referring to an effective resolution of 12 bits as established in (6). The SFDR and THD+N as funtions of frequency are shown in Fig. 17. The desired signal-to-noise ratio of 73 dB is achieved in the full bandwidth up to f_C = 5 MHz. The passband ripple of the SRC is less than ±0.002 dB. For the sampling frequencies $f_{S,1}$ and $f_{S,2}$ from section 2 the overall processing power needed for the SRC is about 548 billion fixed point multiplications and 1067 billion additions per second.

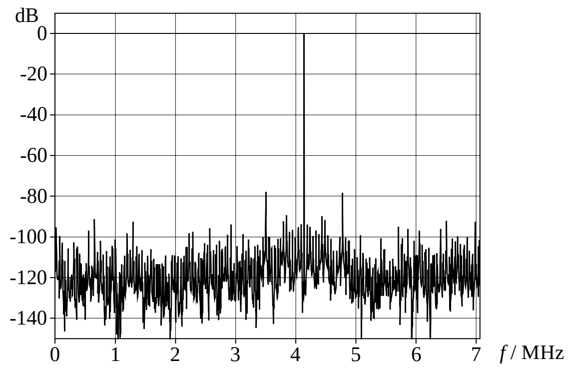

Fig. 16. Magnitude response of a sine-wave output

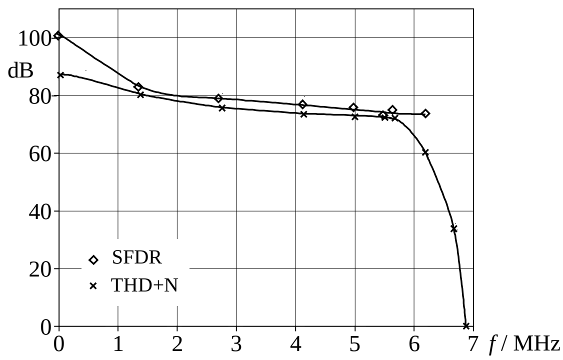

Fig. 17. Total harmonic distortion and noise (THD+N) and spurious free dynamic range (SFDR) of the SRC

6. Conclusion

The completely digital asynchronous sample-rate converter presented in this paper meets the requirements for professional processing of video signals with up to 5 MHz bandwidth and has an effective resolution of 12 bits. Furthermore, its architecture requires low processing power and is well-suited for cost-effective implementation with state of the art digital signal processors and programmable logic devices.

References

[1] D. Wenzel, J. Speidel, "A digital IF modulator for video and associated audio signals", Proc. IEEE Int. Conf. on Communications (ICC), Vancouver, June 1999, pp. 1010-1016.

[2] ITU-R Rec. BT.601-5, "Studio encoding parameters of digital television for standard 4:3 and wide-screen 16:9 aspect ratios", Genf, 1995.

[3] ITU-R Rec. BT.656-3, "Interfaces for digital component video signals in 525-line and 625-line systems operating at the 4:2:2 level of ITU-R Rec. BT.601 (Part A)", Genf, 1995.

[4] ITU-R Rec. BT.799-2, "Interfaces for digital component video signals in 525-line and 625-line systems operating at the 4:4:4 level of ITU-R Rec. BT.601 (Part A)", Genf, 1995.

[5] ITU-R Rec. BT.470-5, "Conventional TV systems", 1998.

[6] D. Wenzel, "A digital TV and audio modulator for digital broadband distribution networks", Dissertation, University of Stuttgart, 1999.

[7] T. I. Laaso, V. Vesa, M. Karjalainen, U. K. Laine, "Splitting the unit delay", IEEE Signal Proc. Magazine, 1996.

[8] T. A. Ramstad, "Digital methods for conversion between arbitrary sampling frequencies", IEEE Trans. ASSP, Vol. 32, No. 3, 1984.

[9] F. Rothacher, "Sample-rate conversion: algorithms and VLSI implementation", Dissertation, TH Zürich, Series in Microelectronics, Vol. 44, Hartung-Gorre, Konstanz, 1995.

[10] E. F. Stikvoort, "Some subjects in digital audio, noise shaping, sample-rate conversion, dynamic range compression and testing. Dissertation, TU Eindhoven, 1992.

[11] "AD1893 low cost sampleport 16-bit stereo asynchronous sample-rate converter – data sheet", Rev. 0, Analog Devices, Norwood, 1995.

[12] P. P. Vaidyanathan, T. Q. Nguyen, "A trick for the design of FIR half-band filters", IEEE Trans. CAS, Vol. 34, 1987.

[13] G. Oetken, et al., "New results in the design of digital interpolators", IEEE Trans. ASSP, Vol. 23, pp. 301-309, 1975.

[14] Burns, et al., "Computer-based exercises for signal processing using MATLAB", Prentice-Hall, New Jersey, 1994.

Dietmar Wenzel was born in Waiblingen, Germany, in 1968. He received his Dipl.-Ing. and Dr.-Ing. degree in Electrical Engineering from the University of Stuttgart, Germany in 1994 and 1999. Since 1994 he has been with the Institute of Telecommunications at the University of Stuttgart as a research and teaching assistant. At the same time he has been closely cooperating with the development division for digital broadband communications systems at Bosch Telecom Backnang. His research interests include digital signal processing with a focus on interfaces for broadband communications systems and sample rate conversion.

Joachim Speidel studied Electrical Engineering at Stuttgart University and received his Dipl.-Ing. and Dr.-Ing. degree in 1974 and 1980. In 1980 he joined Philips as an R & D engineer to work on video data compression, Cable Television, ISDN, optical communications and local loop systems. He has been engaged in various international positions, finally as a Director for R & D. Since 1992, Dr. Speidel is Professor and Director of the Institute of Telecommunications at Stuttgart University. His main research areas are multimedia communication systems, mobile communications and video coding.