A Parallel Equalizer for High-Speed Electronic Dispersion Compensation

Daniel Efinger and Joachim Speidel
Institute of Telecommunications, University Stuttgart, Pfaffenwaldring 47, D-70569 Stuttgart
email: daniel.efinger@inue.uni-stuttgart.de

Abstract *A parallel architecture for linear transversal feed-forward (FFE) and decision feedback equalizers (DFE) is derived and applied to electronic dispersion compensation of a 40 Gbit/s intensity modulated optical transmission system with direct detection (IM/DD).*

Introduction

Electronic dispersion compensation of chromatic (CD) and polarization mode dispersion (PMD) by means of linear transversal FFEs and DFEs has intensively been studied during recent years. Its advantage compared to the more powerful optical compensation techniques or maximum-likelihood sequence estimation (MLSE) in the electrical domain arises from its simple and low cost implementation. Therefore, it can be considered as a favourite candidate for cheap plug and play receivers in future high-speed optical local or metropolitan area networks.

Several research groups and equipment manufacturers have already demonstrated FFE prototypes for 10 and 40 Gbit/s systems which consist of analogue tapped delay lines and which have been fabricated in dedicated SiGe semi-conductor technology [1,2]. So far, no realization of a digital FFE for 10 or 40 Gbit/s systems has been published. One of the reasons is that it is very difficult and expensive to realize a digital chip which is clocked at such high rates. Our idea of a parallel architecture, which allows a trade-off between clock speed and hardware complexity, will mitigate the problem. This approach can be applied to implement plain digital dispersion compensation using FFE and DFE techniques.

Conventional Serial Equalizer Architecture

Fig. 1 shows an example block diagram of a conventional digital FFE with $C=4$ coefficients and a DFE with $D=1$ coefficient. The input signal $y(t)$ is sampled at a rate of $1/T$ and fed to the equalizer. The output $\hat{b}_k$ may for any arbitrary values of C and D be written as the sum of two discrete-time convolutions

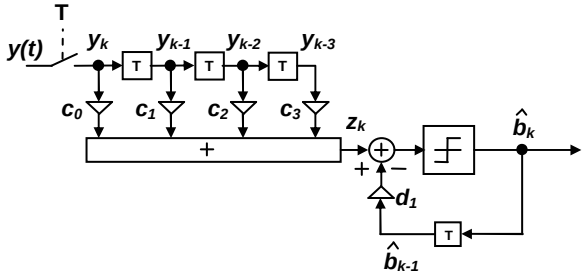

Fig. 1: Conventional serial equalizer structure

$$\hat{b}_k = \sum_{i=0}^{C-1} c_i y_{k-i} - \sum_{j=1}^{D} d_j \hat{b}_{k-j} \qquad (1)$$

with $k = 0,\pm 1,\ldots$ being the discrete time index related to the bit interval T_b, c_i $(i=0,\ldots,C-1)$ being the coefficients of the FFE and d_j $(j=1,\ldots,D)$ being the coefficients of the DFE, respectively. The y_k are the samples of the input signal $y(t)$ at time instants $t = t_0 + kT$. The coefficients of the FFE and DFE are adjusted according to the well-known Least-Mean-Square (LMS) algorithm.

Parallel Equalizer Architecture

For the derivation of the parallel architecture, let us consider the output z_k of the FFE part in Fig. 1

$$z_k = \sum_{i=0}^{C-1} c_i y_{k-i} \qquad (2).$$

The first step to decrease the hardware clock speed by a factor of M is to split up the output z_k into M different output streams z_{Ml-m} in the temporal raster MT with $m = 0,\ldots,M-1$ being the stream index. A new discrete time index l is introduced which is related to the former time index k by $l = k \operatorname{div} M$, where div means integer division.

If we use (2) and express the output streams with respect to the input samples, we get

$$z_{Ml-m} = \sum_{i=0}^{C-1} c_i y_{Ml-m-i} \quad (m=0,\ldots,M-1) \qquad (3).$$

In the same way, we can rearrange the right-hand side of equation (3) and split the convolution sum into M parts with respect to the different input streams $y_{Ml-m-Mj-n}$ $(m,n=0,\ldots,M-1)$, i.e. we replace the summing index i by $Mj-n$. Thus, equation (3) can be rewritten as

$$z_{Ml-m} = \underbrace{\sum_{j=0}^{C_0-1} c_{Mj+0} y_{Ml-m-Mj-0}}_{n=0} + \ldots + \underbrace{\sum_{j=0}^{C_{M-1}-1} c_{Mj+(M-1)} y_{Ml-m-Mj-(M-1)}}_{n=M-1} \qquad (4)$$

$$m=(0,\ldots,M-1); \quad n=(0,\ldots,M-1)$$

with $$C_n = C \operatorname{div} M + \begin{cases} 1 : n \le C \bmod M \\ 0 : n > C \bmod M \end{cases}$$

and the mod-function returning the rest of integer division. Equation (4) can be further transferred into a compact vector notation:

$$z_{Ml-m} = \vec{c}_0^{\,T}\vec{y}_{Ml-m,0} + \ldots + \vec{c}_{M-1}^{\,T}\vec{y}_{Ml-m,(M-1)} \quad (5)$$

with the vectors $\vec{c}_n = [c_n, c_{M+n}, \ldots, c_{M(C_n-1)+n}]^T$ and $\vec{y}_{Ml-m,n} = [y_{Ml-m-n}, y_{Ml-m-M-n}, \ldots, y_{Ml-m-M(C_n-1)-n}]^T$ representing the coefficients and the input samples, respectively, each with temporal raster MT.

Equation (5) gives further insight into the input-output relation of an FFE. The different output streams z_{Ml-m} $(m = 0,\ldots,M-1)$ can be calculated by adding the output of different sub-equalizers given by $\vec{c}_n$ $(n = 0,\ldots,M-1)$. Furthermore, if the input data vectors $\vec{y}_{Ml-m,n}$ $(m,n = 0,\ldots,M-1)$ for the calculation of each output data stream at time instant l are simultaneously available, the output streams z_{Ml-m} $(m = 0,\ldots,M-1)$ can be calculated in parallel at a reduced clock rate of $1/(MT)$. The data troughput is the same as for the serial equalizer.

E.g., assuming $M = 2$, which is also the degree of parallelism, and using the serial FFE of Fig. 1 as reference, equation (5) would lead into two parallel output data streams of the form:

$$z_{2l} = [c_0, c_2]\begin{bmatrix} y_{2l} \\ y_{2l-2} \end{bmatrix} + [c_1, c_3]\begin{bmatrix} y_{2l-1} \\ y_{2l-3} \end{bmatrix}$$
$$z_{2l-1} = [c_0, c_2]\begin{bmatrix} y_{2l-1} \\ y_{2l-3} \end{bmatrix} + [c_1, c_3]\begin{bmatrix} y_{2l-2} \\ y_{2l-4} \end{bmatrix} \quad (6).$$

Equation (6) can be transferred directly into the example block diagram of the parallel equalizer architecture depicted in Fig. 2. The input signal $y(t)$ is available at both input branches by means of an analogue demultipexer structure. Additionally, the conventional DFE part of Fig. 1 is replaced by a so called look-ahead structure with mulitplexer selection, which has already been demonstrated in [3].

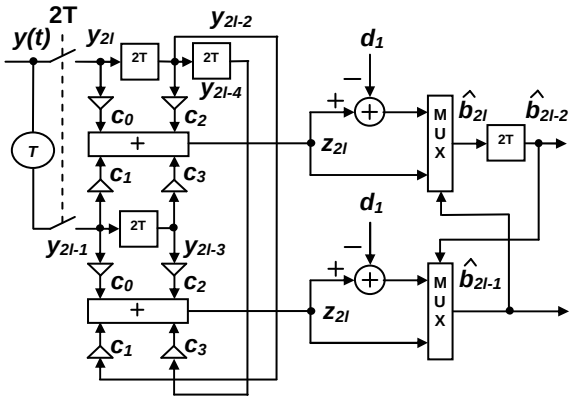

Fig. 2: Parallel equalizer with parallelism of M=2

Verification of the Parallel Equalizer Architecture

In Fig. 3, the required optical signal-to-noise ratio (OSNR) for a bit error rate (BER) of 1.0e-3 is plotted versus residual chromatic dispersion r_d for different equalizer setups with respect to sampling, the number of coefficients and FFE or DFE combination, respectively. Here, FFE means sampling the input signal $y(t)$ at rate of $1/T = 1/T_b$ and FSFFE means sampling at $1/T = 2/T_b$, which is called fractionally spaced equalization. For the parallel equalizers, a degree of parallelism of $M = 4$ was chosen. Assuming IM/DD and a channel bit rate of 42.7 Gbit/s (6.8% FEC-overhead included), the clock rate of the parallel equalizer can be reduced to 10.175 GHz for the FFE and 21.35 GHz for the FSFFE. The optical system model is based upon [4] including a standard single mode fibre affected by chromatic dispersion.

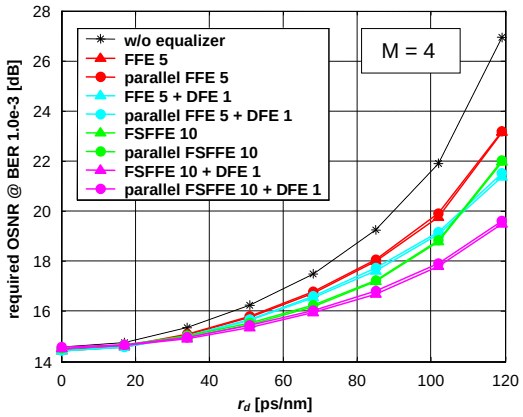

Fig. 3: Simulation results for the parallel equalizer

The simulation results in Fig. 3 prove the concept of the parallel architecture and it can be stated that it performs as well as its serial counterpart. The minor differences between both approaches result from the M - times slower adaptation of the coefficients in the parallel architecture, which might be a drawback.

Conclusion

A parallel architecture which in principle allows digital electronic dispersion compensation has been introduced. By choosing the degree of parallelism appropriately, any trade-off between hardware clock and hardware complexity can be met. As an advantage, smart placing and routing of simple equalizer design macros can be used to build up the parallel architecture. Further research has been started towards a complete digital design using fixed–point arithmetic and a simplified adaptation algorithm.

Acknowledgement

This work was partially funded by the German Federal Ministry of Education and Research (BMBF) within the project EIBONE.

References

1 B. Franz et al, ECOC'05, Vol. 3 (2005), page 333 - 334
2 J. Sewter et al, JNL of Solid-State Circuits, Vol. 41 (2006), page 1919-1929
3 S. Kasturia et al, JNL of Selected Areas in Communications, Vol. 9 (1991), page 711 - 717
4 T. Freckmann et al, PTL, Vol. 18 (2006), page 277-279